Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.031”**

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**.027”**

**Top Material: Al**

**Backside Material: Ti Ni Ag**

**Bond Pad Size = .006 x .008”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .027” X .031” DATE: 6/24/19**

**MFG: ANALOG POWER THICKNESS .006” P/N: AMB421P**

**DG 10.1.2**

#### Rev B, 7/1